

Exercise 2: Laser writer + etching

Location: CMI

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1. Summary

In this exercise you will carry out the first patterning of MoS₂ transferred on top of the device substrate. For this you will use a combination of photolithography, using a laser writer to write a pattern in a photoresist layer. This will be followed by etching in order to remove the surplus material. The goal is to keep only the portions of the material that will form the semiconducting channel in the devices and remove the rest since it could create path for leakage currents and make analysis difficult because you could not be able to say what are the channel dimensions.

This exercise is conceptually very similar to Exercise 3, both use the same equipment for resist coating and exposure, the difference is that here, you use the exposed pattern to etch the material away while in Exercise 3, you deposit the metal for contacts into the exposed areas.

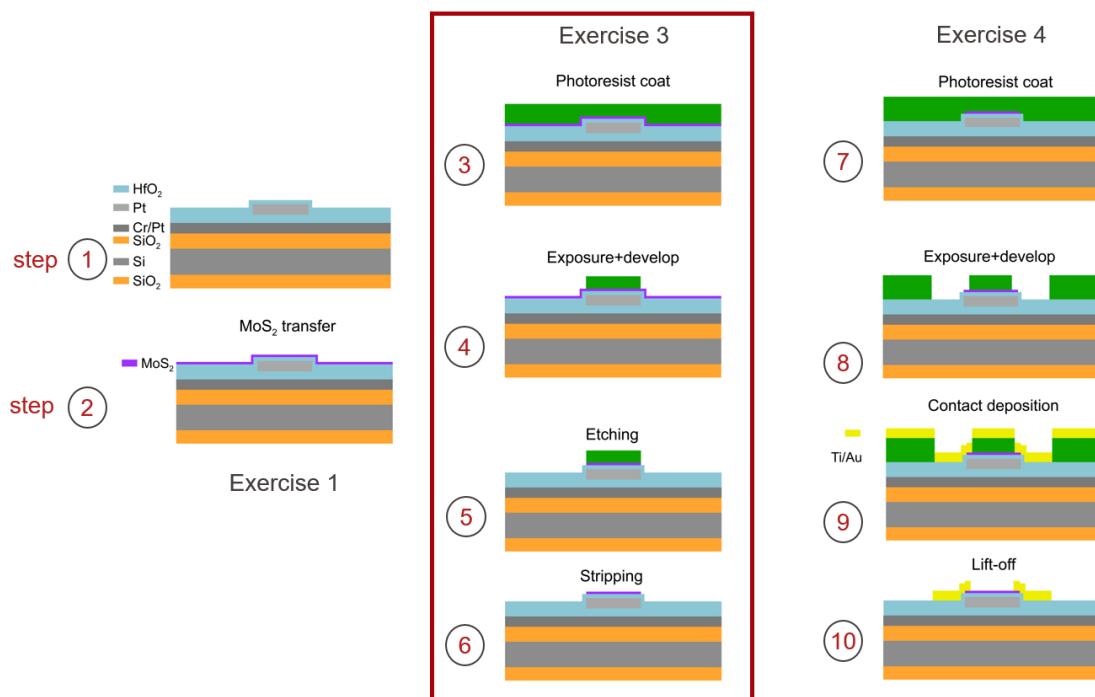


Figure 1. Overview of the complete process flow for the device fabrication in this course. The current exercise is outlined with the red rectangle.

2. Background

A big portion of micro/nanofabrication procedures could be bluntly categorized into procedures for either removing or adding materials. If you are removing materials, this is referred to as etching, if you are adding materials, this is called deposition.

Etching can further be classified into wet and dry etching. For wet etching, we would use a liquid, this can be an aggressive acid like HF (hydrofluoric acid) or a base like KOH or TMAH. Dry etching is performed using gasses, usually at low pressures. Gasses are also often ionized and are in the form of plasma in order to increase their reactivity and to be able to control the direction of etching by using a vertical electric field to accelerate the ions, Figure 2. Some examples are O_2 , Ar, C_2F_6 .

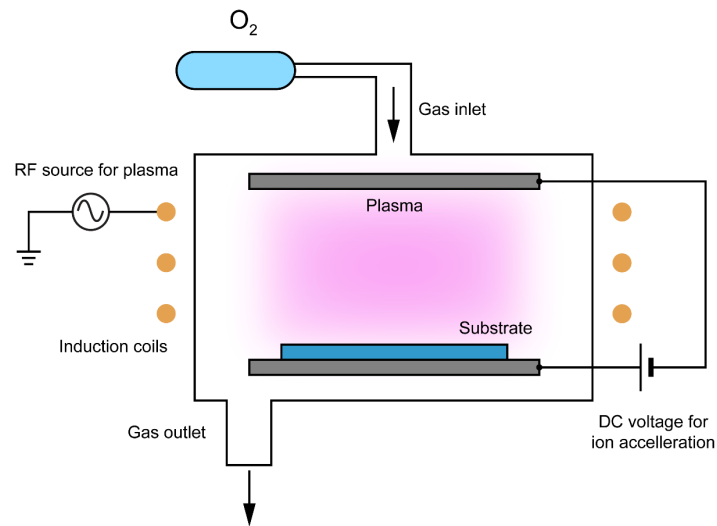


Figure 2. Schematic of a plasma etcher.

When using etching to pattern a material, most of the time, you would like to remove or thin down only portions of your sample/wafer, other portions you would like to keep intact. This is for example the case here because our goal in this exercise is that starting from a relatively large square of MoS_2 , we would like to keep only those parts that will form the transistor and memory device channels for further exercises, and remove everything else. To achieve such a control over the geometry we need to use a so-called etch mask, Figure 2. This is a layer that we put on top of the material. We open windows in this layer and the etching agent will react with the material which is not covered by the mask and will remain intact in the part which is covered. Etch masks are usually removed once the etching is complete, Figure 3. The simplest etch mask to use is a layer of a resist. It is easy to apply, pattern using either photo or e-beam lithography and also easy to remove (“strip”) using organic solvents.

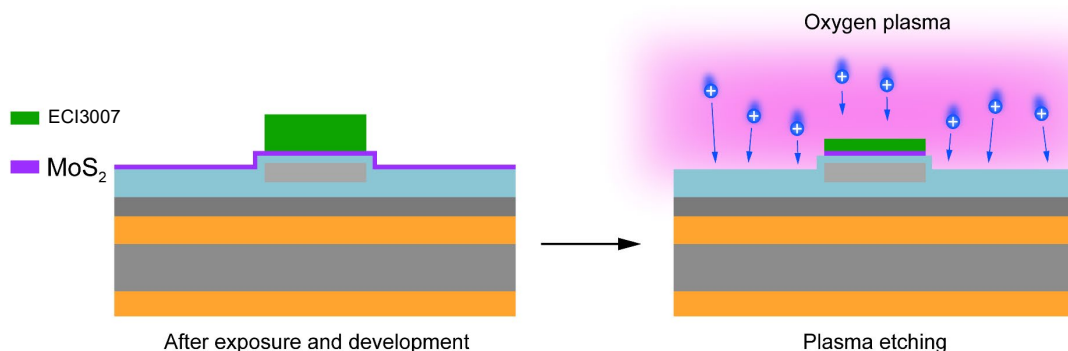


Figure 3. Schematic of the plasma etching process. The photoresist is used as an etch mask.

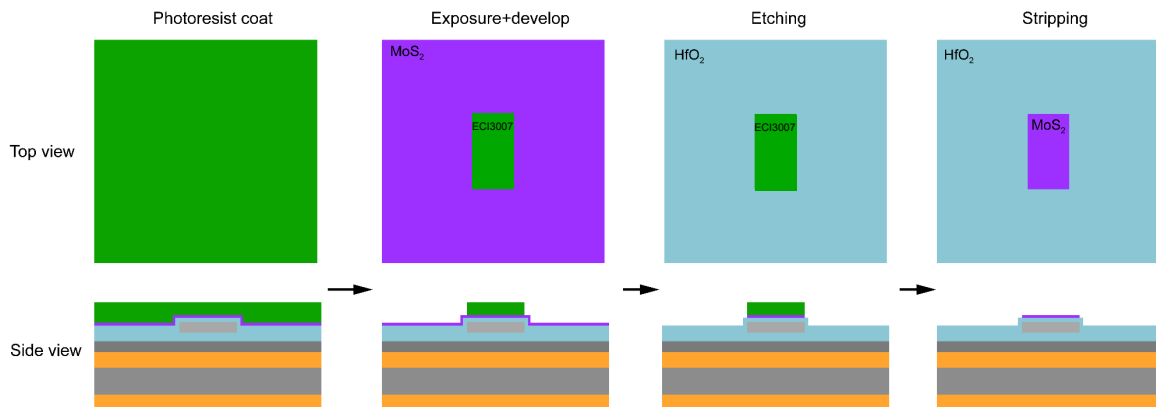


Figure 4. Overview of the process for material patterning via etching.

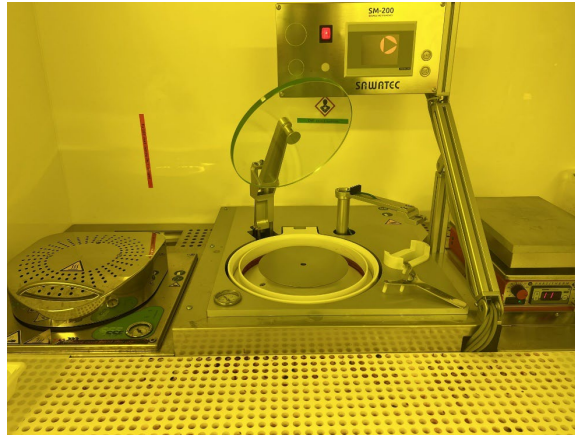
In order to pattern the resist, one can use either light (laser, UV lamp) during photolithography or electrons for e-beam lithography. The interaction with light or the e-beam provokes a chemical change in the resist. Depending on the resist one could either be breaking chains in a polymer or crosslinking the chains. After the exposure, we perform development to remove either the exposed or the unexposed regions of the resist. We distinguish two basic types of resists, depending on how they react to the beam and development. Here, you will use a positive tone resist, meaning that the portions of the resist that are exposed to the laser are removed during the development step. In the case of negative resists, the exposed areas remain during development and the unexposed areas are removed.

A potential drawback of using resists as masks is that they are also easily etched. For example, O₂ plasma that we will use in this exercise etches both MoS₂ and the mask, so there is a risk that for very long etching times, everything would be removed, both the mask and the material, leaving you with a very clean but not very interesting surface. This is however not very likely, since MoS₂ is less than 1 nm thick and the resist is 2 μm thick, so for reasonable etch times, there is little chance of the mask being completely removed.

A comprehensive table with various etchant, material combinations and typical etch rates is given in references [1,2]. As you can see, there is a large selection of etchant materials and procedures. The choice is usually governed by criteria such as the etch rate (speed with which the material is removed), etch selectivity (how fast the material is removed vs. how fast the mask is removed) and whether the process involves toxic etchants. When it comes down to MoS₂ and many other 2D semiconductors, many different dry etching procedures could be used.

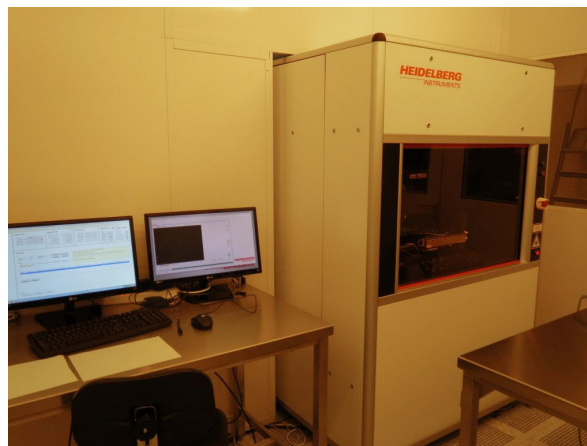
2.1. Description of the equipment used

Sawatec SM-200



Sawatec SM-200 is a manual spin coater. Once the sample loaded by the user on the chuck, it follows the steps of the recipe chosen, varying rotation speed and ramps. Typically, a wafer spin coating starts with a slow step so that resist is evenly spread across the wafer before thinning it down to the desired thickness. For chips, it ends with a short faster step in order to reduce the corner effects.

MLA150



MLA150 is mask-less aligner, a laser writer that makes it possible to write a pattern directly into a photoresist layer, without having to produce a photomask first. This is done by scanning the sample directly under the laser beam. The resolution is limited by the photoresist (length of the molecular chains in the polymer used), light wavelength and numerical aperture of the optics, resulting in a typical resolution of around 1 μm .

TEPLA oxygen plasma dry etcher

Tepla is a compact dry etcher dedicated to using oxygen plasma for removing organic materials from substrates for the main purpose of cleaning. Since MoS_2 can be oxidized at high temperatures (above cca $500\text{ }^\circ\text{C}$), we use it here for etching it. The use of oxygen plasma instead of just oxygen allows us to oxidize MoS_2 at essentially room temperature.

3. Description of experiments and tasks

Following is the overview of the tasks and operations to be carried out in this exercise. The main goal is etch the MoS_2 film into the shape suitable for the realization of transistor, memory and photodetector devices.

3.1. Photoresist coating (Location: Zone 13 – Sawatec SM-200 – Coating)

1. Mount the chip chuck, load the chip and activate the vacuum.
2. Coat the chip with $1\text{ }\mu\text{m}$ thick ECI3007 (positive tone resist) by drop casting and launching the appropriate recipe.
3. Unload the chip and clean the chuck.

3.2. Photoresist exposure (Location: Zone 16, MLA150)

1. Load the chip.
2. Setup the job with the layout conversion and the alignment settings.
3. Perform alignment and expose the chip, with a dose of 120 mJ/cm^2 , defocus 0.

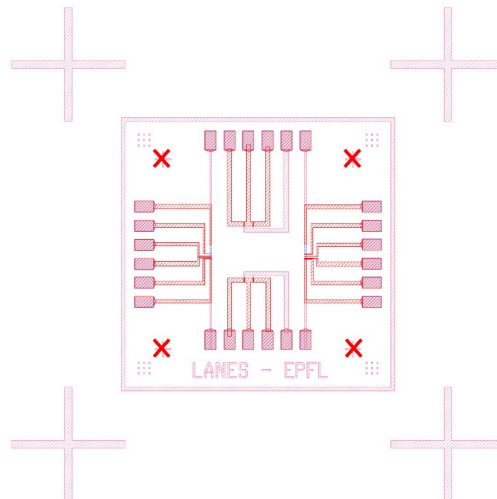


Figure 5. Alignment positions – Manual alignment in the crosses



Figure 6. The pattern to be exposed – MoS₂ Channels with different lengths.

3.3. Development (Location: Zone 13, wet bench)

1. Develop the chip with 1 μm ECI3007 (positive tone resist) using AZ726MIF and rinsing with DI water.
2. Dry the chip using a nitrogen gun.

3.4. Sample inspection

Verify that the sample has been correctly exposed using one of the optical microscopes in CMI.

3.5. Etching (Location: Zone 11, Tepla)

1. Load the chip in the Tepla300 dry etcher.
2. Select recipe 26 for etching the MoS₂.

3.6. Final inspection and resist stripping

1. Put the chip in an acetone bath to remove the photoresist.
2. Inspect the sample and take images for the report.

4. Summary of experiments and tasks

1. Chip coating with the photoresist
2. Photoresist exposure and development
3. Etching of MoS₂

5. Questions for the report

In the report, please show on the following:

1. Optical images of the sample after exposure and etching
2. Justify choice for specific thicknesses, resist and recipes.

6. References

- [1] K. R. Williams and R. S. Muller, *Etch Rates for Micromachining Processing*, J. Microelectromechanical Syst. **5**, 256 (1996).
- [2] K. R. Williams, K. Gupta, and M. Wasilik, *Etch Rates for Micromachining Processing-Part II*, J. Microelectromechanical Syst. **12**, 761 (2003).